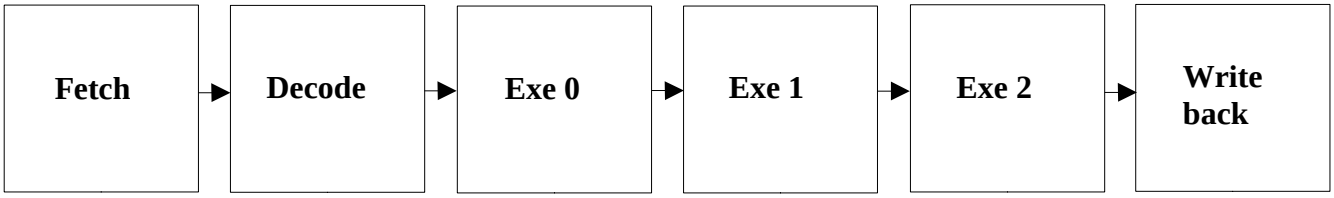
Pipeline of the Core

Overview of the pipeline.



Operations performed in each state

Instruction Fetch
- Instruction is fetched from the instruction memory to the instruction word register.

Instruction Decoding
- 16 bit instructions are expanded to 32 bits.
- Control signals, which are needed in the next cycle are extracted and decoded.
- Execution conditions are verified.
- Register operands are fetched.
- Immediate constants are expanded.
- The target address of a PC relative branch is calculated.

First Execution Cycle
- Condition flags are calculated
- Data memory addresses are calculated.
- Data address validity is checked.
- Instruction address validity is checked.

Second Execution Cycle
- This cycle is needed for multiplication.
- Data memory is accessed during this cycle.

Third Execution Cycle
- This cycle is needed for the *mulhi* instruction, which reads the upper 32 bits of a full 32 x 32 bit multiplication.

Write Back Cycle
- The result of an operation is written back to the register bank.