Interfacing coprocessors

Table 1, Coprocessor interfacing signals.

signal	Direction	purpose/description
	from the	when active
	core side	
COP_EXC[30]:	In	Coprocessor exception. Coprocessor can
$COP_EXC(3) - COP 3$		interrupt the core by pulsing this signal.
$COP_EXC(2) - COP 2$		
$COP_EXC(1) - COP 1$		
$COP_EXC(0) - COP 0$		
COP_PORT(40):	out	Write to cop. Write access to coprosessor
WR_COP		register file.
COP_PORT(39):	out	Read from cop. Read access to coprosessor
RD_COP		register file.
COP_PORT[3837]:	out	Coprocessor index used to address one of the
C_INDX		four possible coprocessors
COP_PORT[3632]:	out	Register index used to select the right register
R_INDX		from the accessed coprocessor register bank.
COP_PORT[310]:	inout	Data to/from the coprocessor.
DATA		
stall	in	Freezes the whole core! This signal does not
		strictly speaking belong to coprocessor interface
		but can be used if no other solution is available.

¹ See document COFFEE_interface about signal type and timing specification.

cop_exc[i] cop_exc[i]