Co-processor interface

COP_PORT(41 downto 0) : Signals of the bus are declared as follows:

cop_port(41) : in : **wait**
cop_port(40) : out : **wr_cop**
cop_port(39) : out : **rd_cop**
cop_port(38 downto 37) : out : **c_index**
cop_port(36 downto 32) : out : **r_index**
cop_port(31 downto 0) : inout : **data**

wait : The signal is active as high. The co-processor which is selected for operation, uses the wait signal to inform the core, that the given task is not ready. In the core pipeline is halted until the signal goes down. This signal is read only when the interface is used in the synchronous mode. In the asynchronous mode this signal is ignored.

wr_cop : Write signal. The signal specifies, that the core writes data to a co-processor.

rd_cop : read signal. The signal specifies, that the core reads data from a co-processor.

c_index : number of the co-processor to work with (2 bits)

r_index : number of the co-processor register to work with (5 bits)

data : Data to or from the selected co-processor.

Two Operating modes: Synchronous and Asynchronous

Synchronous mode

In the synchronous mode, the wait signal is read at every rising edge of the core's clock. The system designer must take into consideration the flip flop's setup and hold times required by the synthesis technology of the core. In other words, in the synchronous operation mode, it is safest to operate the co-processors at a clock rate, which is a multiplicand of the core's clock rate.

Asynchronous mode

In the asynchronous mode it is assumed, that the co-processor can complete the given task in one single clock cycle of the core. The wait signal is completely ignored. The co-processor bus write or read signals are only one clock cycle high (active).