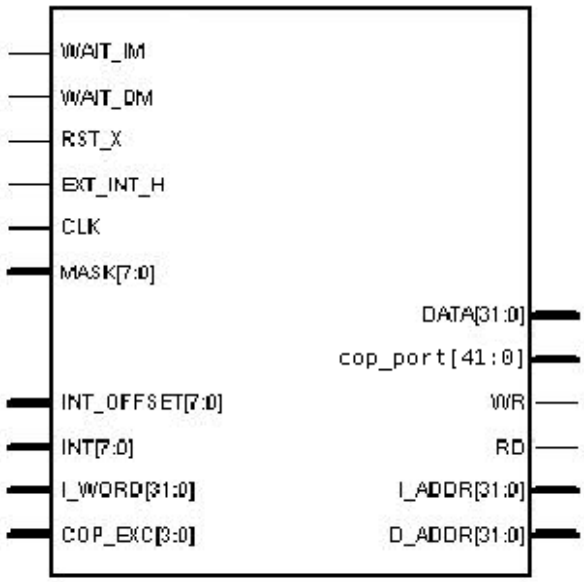
Interface of the Core



Ports of the interface

WAIT_IM : Intruction cache singal to the core. Instruction cache signals to the core to wait in case of a miss.

WAIT_DM : Data cache signal to the core. Data cache signals to the core to wait in case of a miss.

RST_X : Reset signal, active low

EXT_INT_H : External interrupt handler signal. When high, core assumes that an external interrupt handler is present and uses **INT_OFFSET** - signal when calculating handler routine address.

CLK : System clock

MASK[7..0] : Mask vector for external interrupts. Each signal corresponds to one interrupt source. If the signal is high, the exception is enabled, and if the signal is low, the exception is disabled.

INT_OFFSET[7..0] : Interrupt address offset signal. This signal is used if and only if the **EXT_INT_H** - signal is high. With this signal, the interrupt address is calculated as follows:
reg_addr(31 downto 12) & **INT_OFFSET[7 downto 0]** & "0000"

The **reg_addr(31 downto 12)** equals the upper 20 bits of the value in the corresponding interrupt register.
INT[7..0] : Signals from interrupt sources or from the external interrupt handler, if present. Each signal corresponds to one interrupt source. The signal is sensitive to a falling edge. The signal must be high at least 2 clock cycles before the falling edge.

I_WORD[31..0] : Data from the instruction cache.

COP_EXC[3..0] : Co- processor exception signal to the core. Each signal corresponds to one co- processor, and is active when high. The serving mechanism is the same as for interrupts, but the co- processor interrupts are not maskable.

DATA[31..0] : Data to/from the Data-cache.

COP_PORT[41..0] : Co-processor bus. Signalling of the bus is declared as follows:
cop_port(41) <= **wait**
cop_port(40) <= **wr_cop**
cop_port(39) <= **rd_cop**
cop_port(38 downto 37) <= **c_index**
cop_port(36 downto 32) <= **r_index**
cop_port(31 downto 0) <= **data**

wr_cop : write signal
rd_cop : read signal
c_index : number of the co-processor to work with (2 bits)
r_index : number of the co-processor register to work with (5 bits)
data : Data to or from a coprocessor.

WR : Data cache write signal. Active when high.

RD : Data cache read signal. Active when high.

I_ADDR[31..0] : Address of the requested item from the instruction cache.

D_ADDR[31..0] : Address of the requested item from the data cache